

CLAIMS

What is claimed is:

1. A method for providing a connection between a source endpoint and a destination endpoint through a fibre channel switch, the method comprising:
 - 5 receiving FICON frames at the ingress port of a fibre channel switch from a source endpoint, each frame having a header that includes FICON address information;
 - mapping the FICON address information of each received FICON frame to internal address information at the ingress port to provide internal frames;
 - 10 switching the internal frames through the fibre channel switch to an egress port according to the internal address information; and
 - mapping the internal address information of each internal frame to the FICON address information at the egress port for transmission to the destination endpoint.
- 15 2. The method of Claim 1 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein mapping the FICON address information includes mapping the FICON destination address to an internal destination address.
- 20 3. The method of Claim 2 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field.

4. The method of Claim 3 wherein mapping the FICON destination address to the internal destination address includes mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.
5. The method of Claim 3 wherein mapping the internal destination address to the FICON destination address includes mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.
6. The method of Claim 1 wherein the fibre channel switch is one of a plurality of fibre channel switches of a fibre channel switch fabric and further comprising preassigning a chassis address to the fibre channel switch, each chassis having a specific switch address that is different from the preassigned chassis address.
7. The method of Claim 6 further comprising providing in the fibre channel switch a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved chassis address register that includes a physical chassis address of switches within the switch fabric.

8. The method of Claim 7 wherein the FICON address information includes a destination D_ID and mapping the FICON address information includes comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.
9. The method of Claim 8 wherein mapping the internal address information includes comparing the internal chassis address against the reserved address register and inserting the contents of the chassis address register into the destination D_ID.
10. The method of Claim 7 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.
11. The method of Claim 7 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.
12. The method of Claim 7 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.
13. The method of Claim 7 wherein the FICON address information includes a destination D_ID and mapping the FICON address information includes mapping a logical port address in the destination D_ID to a spared port address from a lookup table.

14. The method of Claim 1 wherein the FICON frame includes a cyclic redundancy check (CRC) and wherein mapping the FICON address information to internal address information includes recalculating the CRC and inserting the recalculated CRC into the internal frame.
15. The method of Claim 14 wherein mapping the internal address information to FICON address information includes recalculating the CRC and inserting the recalculated CRC into the FICON frame at the egress port.
16. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:
 - an ingress port for receiving inbound FICON frames from a source endpoint, each frame having a header that includes FICON address information;
 - an address adaptor for mapping the FICON address information of each received FICON frame to internal address information to provide internal frames; and
 - a switch element for switching the internal frames according to the internal address information.
17. The switch of Claim 16 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the address adaptor is operable to map the FICON destination address to an internal destination address.
18. The switch of Claim 17 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field.

19. The switch of Claim 18 wherein the address adaptor is operable to map the FICON destination address to the internal destination address by mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.
20. The switch of Claim 16 further comprising a second address adaptor for mapping the internal address information of each internal frame to the FICON address information to provide outbound FICON frames and an egress port for transmitting the outbound FICON frames to a destination endpoint.
21. The switch of Claim 20 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the second address adaptor is operable to map the internal destination address to a FICON destination address.
22. The switch of Claim 21 wherein the second address adaptor is operable to map the internal destination address to the FICON destination address by mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.

23. The switch of Claim 16 wherein the switch is one of a plurality of fibre channel switches of a fibre channel switch fabric and wherein a chassis address is preassigned to the fibre channel switch, each chassis having a specific switch address that is different from the preassigned chassis address.
- 5 24. The switch of Claim 23 wherein the address adaptor further comprises a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved chassis address register that includes a physical chassis address of the switch.
- 10 25. The switch of Claim 24 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map the FICON address information by comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.
- 15 26. The switch of Claim 25 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.
27. The switch of Claim 25 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.
- 20 28. The switch of Claim 25 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.

29. The switch of Claim 16 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map a logical port address in the destination D_ID to a spared port address from a lookup table.
- 5 30. The switch of Claim 16 wherein the FICON frame includes a cyclic redundancy check (CRC) and wherein the address adaptor is operable to recalculate the CRC and insert the recalculated CRC into the internal frame.
31. In a fibre channel switch, an address adaptor comprising:
- 10 an inbound frame processor for receiving inbound frames from a source endpoint, each inbound frame having a header that includes first address information having a first format, the inbound frame processor including address logic for mapping the first address information of each received inbound frame to second address information having a second format to provide inbound internal frames to a switch fabric; and
- 15 an outbound frame processor for receiving outbound internal frames from a switch fabric, the outbound frame processor including address logic for mapping the second address information of each outbound internal frame to first address information having the first format to provide outbound frames for transmission to a destination endpoint.
- 20 32. The address adaptor of Claim 31 wherein the first format has continuous addressing and the second format has discontinuous addressing.
33. The address adaptor of Claim 31 wherein the first format is FICON format and the second format is an internal format.

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34. The address adaptor of Claim 33 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the address adaptor is operable to map between a FICON destination address to an internal destination address.
35. The address adaptor of Claim 34 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field and wherein the address adaptor is operable to map the FICON destination address to the internal destination address by mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.
36. The address adaptor of Claim 35 wherein the address adaptor is operable to map the internal destination address to the FICON destination address by mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.

37. The address adaptor of Claim 31 for use in a fibre channel switch fabric comprising at least one switch and at least one chassis, wherein all or a portion of the switches in the fabric are preassigned a chassis address, and each chassis has a specific switch address that is different from the preassigned chassis address.
38. The address adaptor of Claim 37 wherein the address logic of the inbound frame processor includes a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved address register that includes a physical chassis address of switches within the switch fabric.
39. The address adaptor of Claim 38 wherein the FICON address information includes a destination D_ID and the address logic is operable to map the FICON address information by comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.
40. The address adaptor of Claim 39 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.
41. The address adaptor of Claim 39 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.
42. The address adaptor of Claim 39 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.

43. The address adaptor of Claim 37 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map a logical port address in the destination D_ID to a spared port address from a lookup table.
- 5 44. The address adaptor of Claim 31 wherein the inbound frame includes a cyclic redundancy check (CRC) and wherein the inbound frame processor is operable to recalculate the CRC and insert the recalculated CRC into the inbound internal frame.
- 10 45. The address adaptor of Claim 44 wherein the outbound frame processor is operable to recalculate the CRC and insert the recalculated CRC into the outbound frame.
46. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:
- 15 means for receiving FICON frames from a source endpoint, each frame having a header that includes a FICON destination address;
- means for mapping the FICON destination address of each received FICON frame to an internal destination address to provide internal frames;
- means for switching the internal frames through the switch according to the internal destination address; and
- 20 means for mapping the internal destination address of each internal frame to the FICON destination address for transmission to the destination endpoint.

47. In an input/output port of a switch, a method of buffer management comprising:
providing a switch element that includes a first buffer;
providing a second buffer;
monitoring the buffer level of the first buffer and the second buffer;
5 upon receipt of a data frame, checking the buffer levels of the first and second buffers;
writing the received data frame to the second buffer if the first buffer is full; otherwise, passing the received data frame to the first buffer if the first buffer is not full and the second buffer is empty; otherwise, reading a data frame
10 from the second buffer and passing the read data frame to the first buffer if the first buffer is not full and the second buffer is not empty.
48. The method of Claim 47 wherein the second buffer is larger than the first buffer.
49. The method of Claim 47 further comprising detecting a start of frame (SOF) in data frames sent to the first buffer, detecting a buffer ready (RDY) signal sent
15 from the switch element upon emptying a data frame from the first buffer, incrementing a first buffer counter upon detection of SOF and decrementing the first buffer counter upon detection of RDY.
50. The method of Claim 47 further comprising detecting a start of frame (SOF) in data frames written to the second buffer, detecting an end of frame (EOF) in data
20 frames read from the second buffer, incrementing a second buffer counter upon detection of SOF and decrementing the second buffer counter upon detection of EOF.

FOI b7c b6 b7c b7d b7e b7f b7g b7h b7i b7j b7k b7l b7m b7n b7o b7p b7q b7r b7s b7t b7u b7v b7w b7x b7y b7z b8a b8b b8c b8d b8e b8f b8g b8h b8i b8j b8k b8l b8m b8n b8o b8p b8q b8r b8s b8t b8u b8v b8w b8x b8y b8z b9a b9b b9c b9d b9e b9f b9g b9h b9i b9j b9k b9l b9m b9n b9o b9p b9q b9r b9s b9t b9u b9v b9w b9x b9y b9z b10a b10b b10c b10d b10e b10f b10g b10h b10i b10j b10k b10l b10m b10n b10o b10p b10q b10r b10s b10t b10u b10v b10w b10x b10y b10z b11a b11b b11c b11d b11e b11f b11g b11h b11i b11j b11k b11l b11m b11n b11o b11p b11q b11r b11s b11t b11u b11v b11w b11x b11y b11z b12a b12b b12c b12d b12e b12f b12g b12h b12i b12j b12k b12l b12m b12n b12o b12p b12q b12r b12s b12t b12u b12v b12w b12x b12y b12z b13a b13b b13c b13d b13e b13f b13g b13h b13i b13j b13k b13l b13m b13n b13o b13p b13q b13r b13s b13t b13u b13v b13w b13x b13y b13z b14a b14b b14c b14d b14e b14f b14g b14h b14i b14j b14k b14l b14m b14n b14o b14p b14q b14r b14s b14t b14u b14v b14w b14x b14y b14z b15a b15b b15c b15d b15e b15f b15g b15h b15i b15j b15k b15l b15m b15n b15o b15p b15q b15r b15s b15t b15u b15v b15w b15x b15y b15z b16a b16b b16c b16d b16e b16f b16g b16h b16i b16j b16k b16l b16m b16n b16o b16p b16q b16r b16s b16t b16u b16v b16w b16x b16y b16z b17a b17b b17c b17d b17e b17f b17g b17h b17i b17j b17k b17l b17m b17n b17o b17p b17q b17r b17s b17t b17u b17v b17w b17x b17y b17z b18a b18b b18c b18d b18e b18f b18g b18h b18i b18j b18k b18l b18m b18n b18o b18p b18q b18r b18s b18t b18u b18v b18w b18x b18y b18z b19a b19b b19c b19d b19e b19f b19g b19h b19i b19j b19k b19l b19m b19n b19o b19p b19q b19r b19s b19t b19u b19v b19w b19x b19y b19z b20a b20b b20c b20d b20e b20f b20g b20h b20i b20j b20k b20l b20m b20n b20o b20p b20q b20r b20s b20t b20u b20v b20w b20x b20y b20z b21a b21b b21c b21d b21e b21f b21g b21h b21i b21j b21k b21l b21m b21n b21o b21p b21q b21r b21s b21t b21u b21v b21w b21x b21y b21z b22a b22b b22c b22d b22e b22f b22g b22h b22i b22j b22k b22l b22m b22n b22o b22p b22q b22r b22s b22t b22u b22v b22w b22x b22y b22z b23a b23b b23c b23d b23e b23f b23g b23h b23i b23j b23k b23l b23m b23n b23o b23p b23q b23r b23s b23t b23u b23v b23w b23x b23y b23z b24a b24b b24c b24d b24e b24f b24g b24h b24i b24j b24k b24l b24m b24n b24o b24p b24q b24r b24s b24t b24u b24v b24w b24x b24y b24z b25a b25b b25c b25d b25e b25f b25g b25h b25i b25j b25k b25l b25m b25n b25o b25p b25q b25r b25s b25t b25u b25v b25w b25x b25y b25z b26a b26b b26c b26d b26e b26f b26g b26h b26i b26j b26k b26l b26m b26n b26o b26p b26q b26r b26s b26t b26u b26v b26w b26x b26y b26z b27a b27b b27c b27d b27e b27f b27g b27h b27i b27j b27k b27l b27m b27n b27o b27p b27q b27r b27s b27t b27u b27v b27w b27x b27y b27z b28a b28b b28c b28d b28e b28f b28g b28h b28i b28j b28k b28l b28m b28n b28o b28p b28q b28r b28s b28t b28u b28v b28w b28x b28y b28z b29a b29b b29c b29d b29e b29f b29g b29h b29i b29j b29k b29l b29m b29n b29o b29p b29q b29r b29s b29t b29u b29v b29w b29x b29y b29z b30a b30b b30c b30d b30e b30f b30g b30h b30i b30j b30k b30l b30m b30n b30o b30p b30q b30r b30s b30t b30u b30v b30w b30x b30y b30z b31a b31b b31c b31d b31e b31f b31g b31h b31i b31j b31k b31l b31m b31n b31o b31p b31q b31r b31s b31t b31u b31v b31w b31x b31y b31z b32a b32b b32c b32d b32e b32f b32g b32h b32i b32j b32k b32l b32m b32n b32o b32p b32q b32r b32s b32t b32u b32v b32w b32x b32y b32z b33a b33b b33c b33d b33e b33f b33g b33h b33i b33j b33k b33l b33m b33n b33o b33p b33q b33r b33s b33t b33u b33v b33w b33x b33y b33z b34a b34b b34c b34d b34e b34f b34g b34h b34i b34j b34k b34l b34m b34n b34o b34p b34q b34r b34s b34t b34u b34v b34w b34x b34y b34z b35a b35b b35c b35d b35e b35f b35g b35h b35i b35j b35k b35l b35m b35n b35o b35p b35q b35r b35s b35t b35u b35v b35w b35x b35y b35z b36a b36b b36c b36d b36e b36f b36g b36h b36i b36j b36k b36l b36m b36n b36o b36p b36q b36r b36s b36t b36u b36v b36w b36x b36y b36z b37a b37b b37c b37d b37e b37f b37g b37h b37i b37j b37k b37l b37m b37n b37o b37p b37q b37r b37s b37t b37u b37v b37w b37x b37y b37z b38a b38b b38c b38d b38e b38f b38g b38h b38i b38j b38k b38l b38m b38n b38o b38p b38q b38r b38s b38t b38u b38v b38w b38x b38y b38z b39a b39b b39c b39d b39e b39f b39g b39h b39i b39j b39k b39l b39m b39n b39o b39p b39q b39r b39s b39t b39u b39v b39w b39x b39y b39z b40a b40b b40c b40d b40e b40f b40g b40h b40i b40j b40k b40l b40m b40n b40o b40p b40q b40r b40s b40t b40u b40v b40w b40x b40y b40z b41a b41b b41c b41d b41e b41f b41g b41h b41i b41j b41k b41l b41m b41n b41o b41p b41q b41r b41s b41t b41u b41v b41w b41x b41y b41z b42a b42b b42c b42d b42e b42f b42g b42h b42i b42j b42k b42l b42m b42n b42o b42p b42q b42r b42s b42t b42u b42v b42w b42x b42y b42z b43a b43b b43c b43d b43e b43f b43g b43h b43i b43j b43k b43l b43m b43n b43o b43p b43q b43r b43s b43t b43u b43v b43w b43x b43y b43z b44a b44b b44c b44d b44e b44f b44g b44h b44i b44j b44k b44l b44m b44n b44o b44p b44q b44r b44s b44t b44u b44v b44w b44x b44y b44z b45a b45b b45c b45d b45e b45f b45g b45h b45i b45j b45k b45l b45m b45n b45o b45p b45q b45r b45s b45t b45u b45v b45w b45x b45y b45z b46a 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51. A switch comprising:
- at least one ingress port for receiving data frames from a source endpoint;
 - a switch element for switching the data frames, the switch element having a first buffer;
 - an adaptor coupled between the ingress port and the switch element and having a second buffer and a buffer controller for monitoring the buffer level of the first buffer and the second buffer wherein upon receipt of a data frame, the buffer controller is operable to check the buffer levels of the first and second buffers and to write the received data frame to the second buffer if the first buffer is full; otherwise, to pass the received data frame to the first buffer if the first buffer is not full and the second buffer is empty; otherwise, to read a data frame from the second buffer and pass the read data frame to the first buffer if the first buffer is not full and the second buffer is not empty.
52. The switch of Claim 51 wherein the second buffer is larger than the first buffer.
53. The switch of Claim 51 wherein the adaptor further includes first buffer logic comprising a first detector for detecting a start of frame (SOF) in data frames sent to the first buffer, a second detector for detecting a buffer ready (RDY) signal sent from the switch element upon emptying a data frame from the first buffer, and a first buffer counter incremented upon detection of SOF and decremented upon detection of RDY.
54. The switch of Claim 51 wherein the adaptor further includes second buffer logic comprising a first detector for detecting a start of frame (SOF) in data frames written to the second buffer, a second detector for detecting an end of frame (EOF) in data frames read from the second buffer, and a second buffer counter incremented upon detection of SOF and decremented upon detection of EOF.

55. A method for providing a connection between a source endpoint and a destination endpoint through a data switch, the method comprising:
- receiving inbound frames at the ingress port of the data switch from a source endpoint, each frame having a header that includes first destination address information;
 - mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames;
 - switching the internal frames through the data switch to an egress port according to the internal destination address information; and
 - mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint.
56. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:
- an ingress port for receiving inbound frames from a source endpoint, each frame having a header that includes first destination address information;
 - an address adaptor for mapping the first destination address information of each received frame to internal address information to provide internal frames; and
 - a switch element for switching the internal frames according to the internal address information.

57. A method for providing a connection between a source endpoint and a destination endpoint through a network of data switches, the method comprising:
- receiving inbound frames at the ingress port of a first data switch in the network from a source endpoint, each frame having a header that includes first destination address information;
 - mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames;
 - switching the internal frames through the network of data switches to an egress port of a second data switch in the network according to the internal destination address information; and
 - mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint.
58. A network of data switches for providing a connection between a source endpoint and a destination endpoint, the network comprising:
- at least one ingress port at a first data switch in the network for receiving inbound frames from a source endpoint, each frame having a header that includes first destination address information;
 - at least one address adaptor at the first data switch for mapping the first destination address information of each received frame to internal address information to provide internal frames;
 - at least another address adaptor at a second data switch in the network for mapping the internal destination address information of each internal frame to the first destination address information to provide outbound frames; and
 - at least one egress port at the second data switch for transmitting the outbound frames to a destination point.